REMARKS

New claims 15 – 21 are pending in the present application. Claims 1 – 14 are cancelled. No new matter is added. Support for the new claims can be found throughout the specification as originally filed, for example in paragraphs [0017] – [0026] and particularly in paragraphs [0021] and [0024] – [0026] and Fig. 4. Reconsideration is respectfully requested.

Rejections under 35 U.S.C. §102

Claims 1-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Pozzi et al. "Automatic Topology-Based Identification of Instruction-Set Extensions for Embedded Processors." Claims 1 - 14 are cancelled.

New claim 15, which is representative of the other claims now in the application recites:

> 15. A process for generating a micro-processor instruction set extension for a processor application, comprising:
>
> generating a data flow graph G(V,E) of nodes V representing primitive operations of the processor application and edges E representing data dependencies of said application;
>
> evaluating subgraphs S of G(V,E) as candidates for an instruction set extension, each said subgraph S having a number of inputs IN(S) and a number of outputs OUT(S), said instruction set extension having a number of available register-file read ports Nin and a number of available register-file write ports Nout;
>
> **wherein said evaluating a subgraph S includes,**
>
> **if OUT(S) is less than or equal to Nout, and**
>
> **if S is convex, and**
>
> **if IN(S) is less than or equal to Nin,**
>
> **then identifying S as a candidate for transformation into an instruction set extension, else disregarding S as a candidate for transformation into an instruction set extension;**
>
> wherein S is convex when no path exists from a node in S to another node in S when said path involves a node that is not in S;
>
> evaluating said identified candidates using a function M(S) as a measure of merit;
>
> transforming said instruction set by adding an instruction set extension representing said identified candidate to said instruction set if said candidate satisfies said function M(S).

Applicants respectfully submit that Applicants' invention as described in the specification and claimed in new claims 14 – 21 provides a completely different process and system for

instruction set extension identification than that described by Pozzi. In particular, Pozzi does not teach or suggest evaluating a plurality of subgraphs according to the number of available register file read ports and write ports, and convexity of the subgraphs. Rather Pozzi considers only Mulitple Inputs Single Output graphs (MISOs) of a maximum kind. The algorithm provided by Pozzi as shown in Pozzi's Figure 1 can be compared and easily distinguished from the process of the present invention as shown, for example, in Applicants' Figure 4.

For at least these reasons, Applicants respectfully submit that independent claims 1 and 21 are patentable over Pozzi. The rejections of claims 1 - 14 under 35 U.S.C. § 102 are moot in view of the amendments herein. Reconsideration is respectfully requested.

CONCLUSION

If any points remain an issue, which the Examiner feels may be best resolved through a telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below. The Examiner is invited and encouraged to telephone the undersigned with any concerns in furtherance of the prosecution of the present application.

Please charge any deficiency as well as any other fee(s) which may become due at any time during the pendency of this application, or credit any overpayment of such fee(s) to Deposit Account No. 50-2896.

Respectfully submitted,

November 20, 2008
Dated:

/Brian L. Michaelis/
Brian L. Michaelis (Reg. No. 34,221)
Customer No. 71130
Attorney for Applicant(s)
SEYFARTH SHAW LLP
World Trade Center East
Two Seaport Lane, Suite 300
Boston, MA 02210
Tel: 617-946-4833
Fax: 617 946-4801
E-mail: bosippto@seyfarth.com